a plurality of contacts including a first plurality of contacts and a second plurality of contacts, said first plurality of contacts located in the second region, and said second plurality of contacts located in the first region such that a smallest distance between adjacent contacts in the first region is different than a distance between the first and second regions, wherein the third region does not have any contacts located therein.

2 1

~~18.~~ The semiconductor package of claim ~~17,~~ wherein the smallest distance between adjacent contacts in the first region is smaller than the distance between the first and second regions.

A1

3 1

~~19.~~ The semiconductor package of claim ~~17,~~ wherein the smallest distance between adjacent contacts in the first region is larger than the distance between the first and second regions.

4 1

~~20.~~ The semiconductor package of claim ~~17,~~ wherein the semiconductor package is a ball grid array package.

5 1

~~21.~~ The semiconductor package of claim ~~17,~~ wherein the plurality of contacts comprises a plurality of contact pads.

12

6 5
22. The semiconductor package of claim 21 further comprising a plurality of solder balls attached to said contact pads.

7 1
23. The semiconductor package of claim 17 wherein each of the second plurality of contacts is contained within a dimensional profile of an integrated circuit coupled to the top surface of the substrate.

8 1
24. The semiconductor package of claim 17 wherein the plurality of contacts are located on the exposed external opposite surface of the substrate.

A1

9 1
25. The semiconductor package of claim 17 wherein said top surface of said substrate has a plurality of bond pads.

10 9
26. The semiconductor package of claim 25 wherein said top surface of said substrate has a ground bus that is connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

11 1
27. The semiconductor package of claim 17 wherein said first plurality of contacts comprises at least five rows of contacts.

12 9
28. The semiconductor package of claim 25 wherein said top surface of said substrate has a power bus that is connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

13 1
29. The semiconductor package of claim 17, wherein said second plurality of contacts is arranged in a four by four matrix.

14
30. A semiconductor package, comprising:

a substrate that includes a top surface having a plurality of bond pads, and an exposed external opposite surface defined by an inner region, an outer region, and a middle region that separates the inner and outer regions;

a plurality of contacts including a first plurality of contacts and a second plurality of contacts, said first plurality of contacts located in the outer region, and said second plurality of contacts located in the inner region such that a first smallest distance between adjacent contacts in the inner region is different than a second smallest distance between the inner and outer regions, wherein the middle region is free of contacts; and

an integrated circuit that is mounted to said top surface of said substrate and coupled to said plurality of bond pads.

15 14
31. The semiconductor package of claim 30, wherein the first smallest distance is smaller than the second smallest distance.

16 14
32. The semiconductor package of claim 30, wherein the first smallest distance is larger than the second smallest distance.

17 14
33. The semiconductor package of claim 30, wherein the semiconductor package is a ball grid array package.

18 14
34. The semiconductor package of claim 30 further comprising a plurality of solder balls attached to said plurality of contacts.

a1 19 14
35. The semiconductor package of claim 30 wherein said top surface of said substrate has a ground bus that is coupled to said integrated circuit and connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

20 14
36. The semiconductor package of claim 30 wherein said top surface of said substrate has a power bus that is coupled to said integrated circuit and connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

21 14
37. The semiconductor package of claim 30 wherein said integrated circuit is enclosed by an encapsulant.

38. The semiconductor package of claim 30 wherein said first plurality of contacts is located outside an outer dimensional profile of said integrated circuit.

39. The semiconductor package of claim 38 wherein said second plurality of contacts is located inside the outer dimensional profile of said integrated circuit.

40. An integrated circuit package for an integrated circuit which has a dimensional profile, comprising:

a substrate that includes a top surface, and an exposed external opposite surface defined by a first region that is substantially equal to the dimensional profile of the integrated circuit, a second region, and a third region that separates the first and second regions; and

a plurality of contacts including a first plurality of contacts and a second plurality of contacts, said first plurality of contacts located within the second region, and said second plurality of contacts located in the first region such that a first smallest distance between adjacent contacts in the first region is smaller than a second smallest distance between the first and second regions, said third region being a contact free region.

41. The integrated circuit package of claim 40, wherein a distance between adjacent contacts in first region is the same as the distance between adjacent contacts in the second region.

26 24

42. The integrated circuit package of claim 40 further comprising a plurality of solder balls attached to said plurality of contacts.

27 24

43. The integrated circuit package of claim 40 wherein said top surface of said substrate has a ground bus that is connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

28 24

44. The integrated circuit package of claim 40 wherein said top surface of said substrate has a power bus that is connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

Amended

Add 31

REMARKS

Applicant submits this Preliminary Amendment canceling claims 1-16 and adding claims 17-44. Examination of the pending claims at the Examiner's earliest convenience is respectfully solicited.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: June 29, 1999.

Helen Lee 06/29/99
Helen Lee *Date*